AF

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kuthi et al.

Serial No.: 09/611,037

Filed: July 6, 2000

For: METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE

Examiner: Alejandro Mulero, L.

Art Unit: 1763

Atty. Docket No.: LAM1P077A

Date: February 15, 2006

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on **February 15, 2006**.

Signed: _____

Sylvia Castillo

REINSTATEMENT OF APPEAL AND TRANSMITTAL OF REPLY BRIEF

Commissioner for Patents
Mail Stop: Appeal Brief- Patents
Alexandria, VA 22313-1450

Sir:

Applicants hereby reinstate the Appeal in this matter. The Notice of Appeal was filed on November 29, 2004, and an Appeal Brief was filed on March 3, 2005. Following Applicants' Appeal Brief, a non-final action was mailed on May 13, 2005. Applicants filed a Supplemental Appeal Brief on September 13, 2005. Following Applicants Supplemental Appeal Brief, an Examiner's Answer was mailed on December 15, 2005. Appellants submit this Reply Brief in response to the Examiner's Answer dated December 15, 2005.

Applicants assert and/or enclose the following:

The Notice of Appeal fee has already been paid.

The fee for filing the Appeal Brief has already been paid.

Appellants submit this Reply Brief in response to the Examiner's Answer dated December 15, 2005.

Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Months	Large Entity	Small Entity
☐ one	$120.00	$60.00
☐ two	$450.00	$225.00
☐ three	$1,020.00	$510.00

If an additional extension of time is required, please consider this a petition therefor.

Total Fees Due:

Notice of Appeal Fee	$ 0
Extension Fee (if any)	$ 0
Total Fee Due	$ 0

Enclosed is Check No. _____ in the amount of $___.

Charge any additional fees or credit any overpayment to Deposit Account No. 50-0850, (Order No. LAM1P077A).

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

Lie-Yea Cheng, Patent Agent
Registration No. 52,732

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
(408) 749-6900
Customer No. 25920

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE KUTHI, ET AL.

Application for Patent

Filed July 6, 2000

Application No. 09/611,037

Examiner: Luz L. Alejandro Mulero

Art Unit: 1763

FOR:

METHOD FOR IMPLEMENTING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE

REPLY BRIEF

CERTIFICATE OF MAILING

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Signed: _____
Sylvia Castillo

MARTINE PENILLA & GENCARELLA, LLP
Attorneys for Appellants

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I. STATUS OF CLAIMS

The status of the claims remains the same as outlined in the Appeal Brief. A total of 40 claims were presented during the prosecution of the present application. Applicants canceled claims 1-13 and 22-32. Applicant appeals the final rejection of claims 14-21 and 33-40. A copy of the claims is attached in Appendix A.

II. GROUNDS OF REJECTION TO BE REVIEW ON APPEAL

The grounds for rejection to reviewed on appeal are as follows:

A. Claims 33-35, 37-38, and 40 were finally rejected under 35 USC §103(a) as being unpatentable over Tomita et al. in view of admitted prior art (APA); and

B. Claims 14-21, 36, and 39 were finally rejected under 35 USC §103(a) as being unpatentable over admitted prior art in view of Chang et al., or alternatively, by Chang et al. in view of admitted prior art (APA).

III. ARGUMENT

A. Claims 33-35, 37-38, and 40 are not rendered obvious by the patent to Tomita et al. in view of admitted prior art (APA).

In the Examiner's Answer, the Examiner submits that the disclosure in Appellants' specification establishes a clear relationship between the size of the openings and the plasma sheath present within the openings. Appellants generally agree with this statement. Indeed, to cause a first surface of a plasma sheath to shift into electrode openings, the size of the openings must be larger than the plasma sheath thickness. However, plasma sheath thickness is affected by a number of parameters, including pressure, power, and chemistry, as stated in the Declaration filed under 37 CFR 1.132 on March 3, 2005. For the exemplary system described by Appellants, the size of the openings must be larger than 0.5 mm. However, it does not mean any showerhead with openings greater than 0.5 mm would cause the plasma sheath to shift into the electrode openings. For a showerhead in a reactor with different pressure, power, and chemistry from the exemplary system described by the Appellants, the plasma sheath thickness could be larger than 0.6 mm or 0.8 mm. For such a reactor, the plasma sheath would not necessarily shift into the electrode openings, even when the electrode openings are greater than 0.5 mm. This argument also supports our previous statement that "The size of the electrode openings is but one parameter of many features of the present claimed method. It is not a valid assumption to conclude that any electrode having electrode openings of a particular size (such as >0.5 mm), will result in a plasma shift into the electrode openings." Therefore, the case of inherency is not established.

In addition, Tomita et al. does not describe "providing a processing chamber, ..., and a pair of RF power sources," as defined in independent claims 33 and 37. Tomita et al. describes a reactor with aN RF power source 12 connected to the shower electrode 3 and a DC power source E housed in the chuck electrode 61. The DC power E is likely used to induce electrostatic force to chuck the substrate. Tomita et al.'s reactor does not include a pair of RF power sources. The pair of RF power sources (118a and 118b) described in the Appellants' invention provide a shifted sinusoidal voltage wave 302' of the Appellants' electrode design. The pair of RF power sources affect the sinusoidal RF voltage waveforms (both in magnitude and

frequency) shown in Figure 4A and would consequently affect the magnitudes of current and time in Figure 4B and bias versus area ratio of Figure 5. In contrast, Tomita et al.'s single RF power source (primarily for generating plasma) and single DC power source would generate a different bias voltage plot from voltage wave 302' of Figure 4A.

The Examiner states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Tomita et al. so as to include two RF power sources two RF power sources coupled to the upper and lower electrodes, as described in APA. In page 5, lines 7-16 of the Appellants' specification, the Appellants have described that increasing the RF bias power may change the chemical composition and may fail to perform the desired etching. Therefore, it would not be obvious that one skilled in the art to modify Tomita et al.'s system to replace the DC power source E with a RF power source 118b to achieve Tomita et al.'s desired etching. Additionally, Tomita et al. uses 400 KHz RF power to generate plasma. While the examples used in the APA is using 27 MHz for generating plasma and using 2 MHz for generating a bias voltage. If a RF power source is to be connected to the chuck of Tomita et al.'s reactor, it would not be obvious to one skilled in the art to know what frequency should be used without further engineering development. To establish a *prima facie* case of obviousness based on a combination of references, there must be some suggestion or motivation, either in references or in the knowledge generally available to one having ordinary skill in the art, to combine the references in the manner proposed. As explained above, the Examiner has not established a *prima facie* case of obviousness against the claimed subject matter because one having ordinary skill in the art would not have combined Tomita et al. with APA in the manner proposed by the Examiner.

As a consequence, Claims 33-35, 37-38, and 40 are not rendered obvious by the patent to Tomita et al. in view of admitted prior art (APA).

B. Claims 14-21, and 33-40 are not rendered obvious by admitted prior art in view of the patent to Chang et al., or alternatively, by the patent to Chang et al. in view of admitted prior art (APA).

Similar to the rejections addressed above in section "A," the Office has cited the structure of the apparatus described by Chang et al., and asserted that it teaches the method claimed by Applicants. As stated previously in section A, the size of the gas feed holes, or electrode openings, is but one parameter of many parameters in one of a plurality of etch processes. It is not a valid assumption to conclude that any electrode having electrode openings of a particular size (such as >0.5 mm), will result in a plasma shift into the electrode openings." Therefore, the case of inherency is not established.

In addition, Chang et al. describes a plasma deposition chamber, which is used to deposit film on the substrate surface. In contrast, the Appellants' invention describes a plasma etching chamber, which is used to remove film or material layer on the substrate surface. The plasma in a PECVD (plasma enhanced chemical vapor deposition) chamber is different from the plasma in a plasma etching chamber in many ways, for example the ion energy is typically lower in a PECVD chamber than an etching chamber. Therefore, in a typical PECVD chamber, such as the one described by Chang et al., the substrate is not held by a chuck and is not biased. The Examiner's statement that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Chang et al. by holding the wafer with a chuck and by coupling RF power to the chuck in order to generate a bias voltage within the plasma region is not correct.

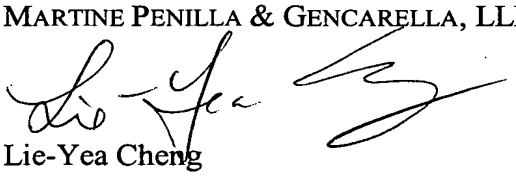
To establish a *prima facie* case of obviousness based on a combination of references, there must be some suggestion or motivation, either in references or in the knowledge generally available to one having ordinary skill in the art, to combine the references in the manner proposed. It would not have been obvious t one skilled in the art to combine the teachings of a deposition chamber with the teachings of an etching chamber. Therefore, the Examiner has not established a *prima facie* case of obviousness against the claimed subject matter because one having ordinary skill in the art would not have combined Chang et al. with APA in the manner proposed by the Examiner.

As a consequence, Claims 14-21, and 33-40 are not rendered obvious by the admitted prior art in view of the patent to Cheng et al., or alternatively, by the patent to Chang et al. in view of admitted prior art.

IV. CONCLUSION

For the foregoing reasons, the rejections of claims 14-21, and 33-40 under 35 U.S.C. §103(a) are improper. Appellants request that the Board of Patent Appeals and Interferences reverse the rejections and remand the case to the Examiner for allowance.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP



Lie-Yea Cheng
Reg. No. 52,732

MARTINE PENILLA & GENCARELLA, LLP
710 Lakeway Drive, Suite 200
Sunnyvale, California 94085
Customer Number 25920

APPENDIX A

CLAIMS ON APPEAL

14. In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber being in an operational state and including a support chuck for holding the semiconductor wafer, a pair of RF power sources, and a top electrode, a method for processing a semiconductor wafer through plasma etching operations, comprising:

striking a plasma in a plasma region of the chamber; and

generating an increase in bias voltage directed at a wafer surface of the semiconductor wafer and a decrease in bias voltage directed at the top electrode, the top electrode having a center region, a first surface and a second surface, the first surface having an inlet that is configured to receive processing gases from a source that is external to the chamber and flow the processing gases into the center region, the second surface having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface which is located over the wafer surface of the semiconductor wafer,

wherein when a plasma is struck in the plasma region defined between the second surface and the wafer surface, the plasma defines a first plasma sheath surface having a first plasma sheath surface area that is proximate to the wafer surface and a second plasma sheath surface having a second plasma sheath surface area that is proximate to the second surface, the second plasma sheath surface area being greater than the first plasma sheath surface area.

15. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

causing the second plasma sheath surface having the second plasma sheath surface area to shift into the electrode openings of the second surface of the top electrode, the electrode openings being at least 0.5 mm or greater in diameter and the gas feed holes having a diameter of about 0.1 mm.

17. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the second surface and the wafer surface.

19. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 18, further comprising:

fixing a separation between the second plasma sheath surface having the second plasma sheath surface area and the second surface of the top electrode at between about 0.5 mm and about 5 mm.

21. The method for processing a semiconductor wafer through plasma etching operations as recited in claim 14, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath surface area is greater than the first plasma sheath surface area.

33. A method of processing a semiconductor wafer, comprising:

providing a processing chamber, the processing chamber being in an operational state and including a top electrode, a wafer support chuck having the semiconductor wafer positioned thereon, and a pair of RF power sources;

striking a plasma within a plasma region of the processing chamber; and

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode,

wherein the plasma sheath defines the first surface of the plasma sheath next to the top electrode and a second surface of the plasma sheath over a surface of the semiconductor wafer.

34. The method of processing a semiconductor wafer as recited in claim 33, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of the second surface of the plasma sheath.

35. The method of processing a semiconductor wafer as recited in claim 33, further comprising increasing a bias voltage over the surface of the semiconductor wafer while slightly decreasing the bias voltage over a surface of the top electrode and without increasing a plasma density.

36. The method of processing a semiconductor wafer as recited in claim 33, wherein the top electrode has a center region, a first surface and a second surface, the first surface of the top electrode having an inlet that is configured to receive processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the second surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the second surface of the top electrode which is located over the surface of the semiconductor wafer.

37. A method for high aspect ratio semiconductor etching, comprising:

providing a plasma etch processing chamber, the plasma etch processing chamber including a top electrode, a wafer support chuck, and a pair of RF power supplies, and the plasma etch processing chamber being configured in an operational state;

striking a plasma in a plasma region of the plasma etch processing chamber, the plasma region being defined between an electrode surface of the top electrode and a wafer surface of a wafer positioned on the wafer support chuck;

causing a first surface of a plasma sheath to shift into electrode openings of the top electrode, the first surface of the plasma sheath being proximate to the top electrode; and

increasing a bias voltage over the wafer surface while decreasing the bias voltage over the electrode surface of the top electrode and without increasing a plasma density.

38. The method for high aspect ratio semiconductor etching of claim 37, further comprising increasing an ion bombardment energy on the wafer surface.

39. The method for high aspect ratio semiconductor etching of claim 37, wherein the top electrode has a center region, a first surface and the electrode surface, the first surface of the top electrode having an inlet that is configured to receive processing gases from a source that is external to the processing chamber and to flow the processing gases into the center region, the electrode surface of the top electrode having a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings being configured to define the electrode surface of the top electrode which is located over the wafer surface.

40. The method for high aspect ratio semiconductor etching of claim 37, wherein a surface area of the first surface of the plasma sheath is greater than a surface area of a second surface of the plasma sheath, the second surface of the plasma sheath being defined proximate to the wafer surface.